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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,004	12/30/2003	Yong Woo Shin	2013P149	9937

8791 7590 05/09/2006

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EXAMINER	
JOHNSTON, PHILLIP A	

ART UNIT	PAPER NUMBER
2881	

DATE MAILED: 05/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/750,004	SHIN ET AL.	
	Examiner	Art Unit	
	Phillip A. Johnston	2881	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3-2004; 8-2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1. This Office Action is submitted in response to amendment dated 3-2-2006, wherein claim 1 was amended. Claims 1-10 are pending.

2. The examiner agrees with the remarks filed 3-2-2006 in particular that, Kawamura (686) does not anticipate the applicant's claim 1, and the § 102 (b) rejection is hereby withdrawn.

Claims Rejection – 35 U.S.C. 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-4 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent Pub. No. 5,601,686 to Kawamura, and Hashiguchi, U.S. Patent No. 6,461,986.

Kawamura (686) as applied in the previous Office Action, discloses nearly all the limitations of claims 1-4, but fails to teach;

(a) Pre-bake and post-bake chambers, as recited in claim 2;

(b) An alignment chamber, as recited in claim 3; and

(c) A cooling chamber, as recited in claim 4.

However, Hashiguchi (986) discloses the use of aligner 4, pre-bake chambers 23 and 24; post-bake chambers 28 and 29; and cooling units 21,26, and 27, as recited in claims 2-4. See Column 7, line 6-58.

Therefore it would have been obvious to one of ordinary skill in the art that the electron beam lithography system of Kawamura (686) can be modified to use the pre-bake, post-bake, and cooling process chambers of Hashiguchi (986), to provide means for carrying a wafer into/out of a processing station in which various kinds of processing and treatment units each for performing predetermined processing or treatment steps, thereby providing a system structured to process a plurality of wafers concurrently at the same time..

5. Claims 5-10 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Kawamura (686) and Nakasuji, U.S. Patent No. 6,593,152.

Kawamura (686) as applied above fails to teach the use of ;

(a) A Robot wafer handler/loader, as recited in claim 5;

(b) A vibration isolator, as recited in claims 6 and 7;

(c) Slot valves and flexible adaptors, as recited in claims 8 and 9; and

(d) A vacuum system for maintaining pressure in the lithography chambers, as recited in claim 10.

However, Nakasuji (152) discloses;

(a) A Robot wafer handler/loader, as recited in claim 5. See Column 7, line 51-65; and Column 12, line 62-65;

(b) Vibration isolator 37 mounted on base frame 36, as recited in claims 6 and 7. See Column 9, line 31-54;

(c) Gate (slot) valves 27,45, and 46, and Flexible pipes (adaptors) 21-2, 27-2, as recited in claims 8 and 9. See Column 10, line 38-69; and Column 30, line 27-53 respectively;

(d) A vacuum system for maintaining atmospheric pressures in the test chambers at 10^{-6} torr, as recited in claim 10. See Column 9, line 50-67; and Column 10, line 1-16.

Therefore it would have been obvious to one of ordinary skill in the art that the electron beam lithography system of Kawamura (686) can be modified to use the lithography manufacturing equipment of Nakasuji (152), to provide a robot for automatic wafer loading; a vibration isolator to block vibrations from the floor; a vacuum system for maintaining a desired pressure in each chamber; and a gate valve for selectively blocking a communication between adjoining chambers; thereby providing a loading chamber structure with improved throughput.

Examiners Response to Arguments

6. Applicant's arguments filed 3-2-2006 have been fully considered but they are not persuasive.

Argument 1

Applicant states that "Applicant has addressed Kawamura above in section I regarding amended claim 1. As asserted above, Kawamura does not teach, disclose

or suggest [a plurality of wafers are respectively loaded into the plurality of electron beam lithography chambers so as to drive the electron beam lithography chambers at the same time, and the plurality of wafers are processed in the plurality of electron beam lithography chambers at the same time.] "

The applicant is respectfully directed to Kawamura (686), Column 9, line 57-67; and Column 10, line 1-26, which state; In another process chamber (not shown), there may be performed a dry cleaning process using plasma gas, an ashing cleaning process by irradiation of shortwave light, a cleaning process by the supply of chlorine gas and irradiation of shortwave light, a thin film deposition process using a chemically vaporized gas, a lithography process for reduction projection of a mask pattern using ultraviolet light, a patterning process for directly patterning in a specified atmosphere by charged particle beams, a process for depositing a thin film in a pattern by irradiating energy beams such as ultraviolet light or electron beams in a pattern while supplying a specified reactive gas, or a process of diffusing atoms in a pattern. In addition, gases can be changed and combined, and the process can be made while the processing state of the surface of the substrate is measured. Moreover, another process may be used to measure and analyze the surface of the substrate.

Since the process chambers 2 capable of applying various processes are disposed around the transport chamber 1 by way of the interface means 3 of the present invention, a substrate can be smoothly transported between the process chambers and then processed without any contamination of each atmosphere and

the substrate while the different atmospheric conditions of the process chambers and the transport chamber are kept as they are. In particular, since the substrate can be transported without any change in the atmospheric conditions of the process chambers and the transport chamber, it becomes possible to eliminate the time required for the exhaust and pressure-setting for equalizing the atmospheric conditions of the chambers from and to which the substrate is transported. As a result, the throughput is improved and the contamination of the substrate is reduced; accordingly, the semiconductor device having a high performance can be manufactured at a high yield. Moreover, the reduction in the contamination of the substrate decreases the number of the cleaning process steps, which reduces the number of the process steps of the semiconductor device, thereby further improving the throughput.

The examiner has interpreted that, various semiconductor processes, including electron beam lithography can be performed in any of the independently controlled process chambers in accordance with Kawamura (686), and that it would have been obvious to one of ordinary skill in the art that, the cluster of Kawamura (686) is capable of being used to perform plural electron beam lithography processes in plural chambers at the same time.

Conclusion

7. The Amendment filed on 3-2-2006 under 37 CFR 1.131 has been considered but is ineffective to overcome the references cited in the Office Action mailed 9-30-2005.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications should be directed to Phillip Johnston whose telephone number is (571) 272-2475. The examiner can normally be reached on Monday-Friday from 6:30 am to 3:00 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiners supervisor John Lee can be reached at (571) 272-2477. The fax phone number for the organization where the application or proceeding is assigned is 571 273 8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NIKITA WELLS
PRIMARY EXAMINER
05/05/06

PJ
May 2, 2006